

DESCRIPTION

Demonstration circuit 1562A is an engineering tool to design and evaluate the LTC699X-X family of TimerBlox circuits. The center section of the board contains a pre-configured TimerBlox function. DC1562A comes in twelve timing function variations as outlined in Table 1.

Surrounding the center board is a "playground" prototyping area. The prototyping area has pads for Dip-8, S8, MS8, or S6 packages with breadboarding connections to each pin and two convenient power buses and ground bus surrounding the entire area. This area is for conditioning signals to control the timer function and for adding loads controlled in time.

The center part of the board can be broken away on its own as a convenience for adding a timing function to a pre-existing circuit. For application flexibility a provision is made for buffering and inverting the output of the timer. An optional NC7W04P6X SC70 package dual inverter can be added at U2 to provide this functionality.

**Design files for this circuit board are available.
Call the LTC factory.**

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USING THE DEMO BOARD

To understand the simplicity and flexibility of the TimerBlox function download the appropriate data-sheet from the LTC Website, www.linear.com for the device to be used. To change the board from the supplied default configuration is a simple matter of determining a few new resistor values. Simply select a pair of resistor values for the DIV value from the data sheet DIV Table, calculate the value of R_{SET} required, replace the resistor on the board, apply power, and go! Single supply power between 2.25V and 5.5V and ground must be supplied directly to the center board.

The outer prototyping section of the board can be used with Single or Dual supplies as required.

When using the prototyping area, the outermost trace, which is ground, must be connected (hand wired) to the ground on the center board section. All input and output holes are sized for 65 mil. turret terminals, or wires can be soldered in the holes directly.

To experiment with different timer configurations requires changing resistor values on the center board. The through hole resistor lead holes can take pressed in IC socket pins from DIP sockets or resistors can soldered directly in the holes. Pads for 0805 surface mount resistors are also included at each position where a leaded resistor could be used. Pads are also included for three 25-turn trim

LTC699X

pots which can be used to replace R_{SET} (R8) for master oscillator frequency adjustment, PSF in (R10) for voltage controlled options, and R_{DEV} (R7) for frequency divider control to permit real-time adjustments while running.

A TimerBlox part, decoupling cap and a bulk decoupling 10 μ F Tantalum cap are already placed on the board. Resistors are also provided to configure each device for a representative function to start evaluating these unique timing functions.

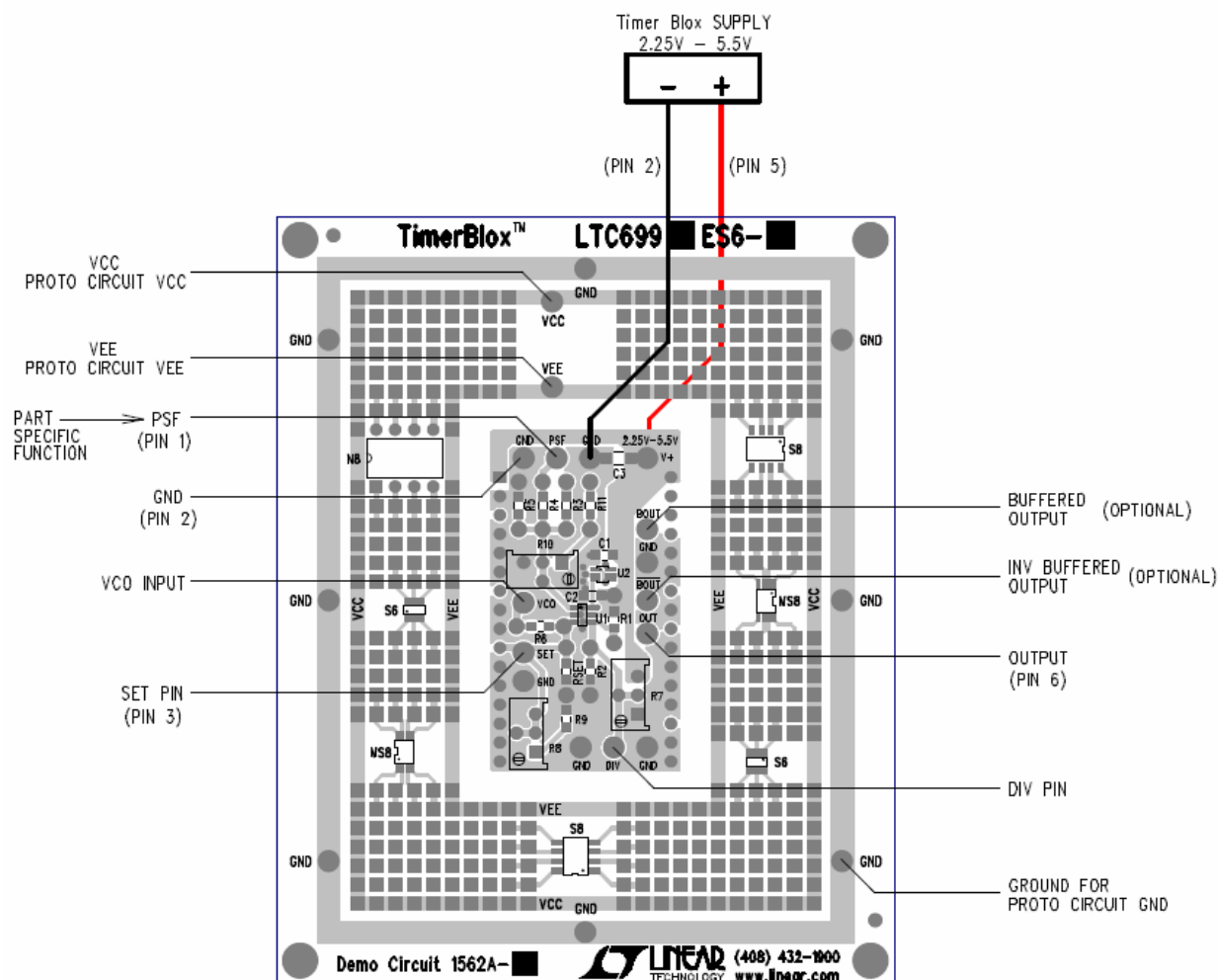
TABLE 1. STANDARD CONFIGURATION FOR EACH VERSION

Demo Board Number	LTC Part Number	Part Marking	Function	Configured Function
DC1562A-A	LTC6990	LTDWW	HF OSC	1KHz to 10 KHz Voltage Controlled Oscillator
DC1562A-B	LTC6991	LTDWY	LF OSC	1 Hz (1Sec) Fixed Frequency Oscillator
DC1562A-C	LTC6992-1	LTDXB	PWM	10KHz 0 – 100% Duty Cycle PWM
DC1562A-D	LTC6992-2	LTDXD	PWM	10KHz 5 – 95% Duty Cycle PWM
DC1562A-E	LTC6992-3	LTFCQ	PWM	10KHz 0 – 95% Duty Cycle PWM
DC1562A-F	LTC6992-4	LTFCV	PWM	10KHz 5 – 100% Duty Cycle PWM
DC1562A-G	LTC6993-1	LTDXG	One-Shot	RET* 100 ms Positive Output Pulse
DC1562A-H	LTC6993-2	LTDXJ	One-Shot	RET* Re-Triggerable 100 ms Positive Output Pulse
DC1562A-I	LTC6993-3	LTFMH	One-Shot	FET** Positive 100 ms Output Pulse
DC1562A-J	LTC6993-4	LTFMK	One-Shot	FET** Re-Triggerable 100 ms Positive Output Pulse
DC1562A-K	LTC6994-1	LTFCV	Delay	Output Falling Edge Delayed 100 ms from Input Falling Edge
DC1562A-L	LTC6994-2	LTFCX	Delay	Output Rise/Fall Edges Delayed 100 ms from Input Rise/Fall Edges

* Rising Edge Triggered

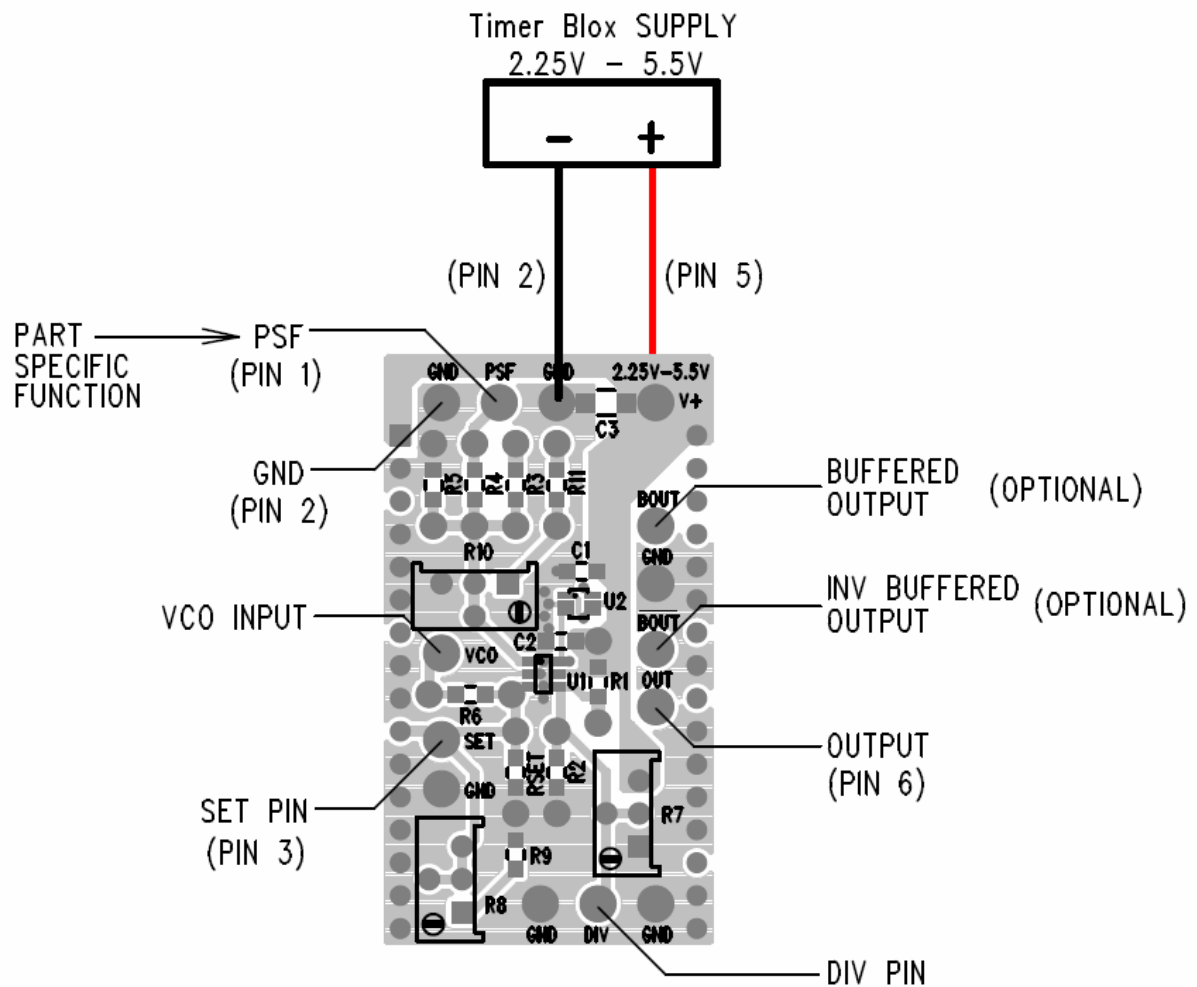
** Falling Edge Triggered

DC1562A-X EXTERNAL CONNECTION DIAGRAM



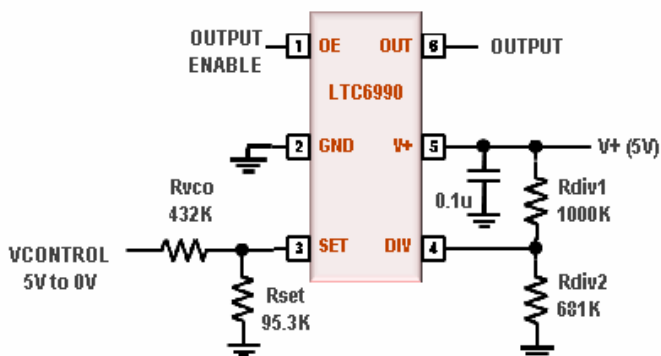
NOTE: TIMER SUPPLY AND GROUND ARE NOT CONNECTED TO THE PROTO CIRCUIT SUPPLY TRACES.

DC1562A-X CENTER BOARD CONNECTION DIAGRAM

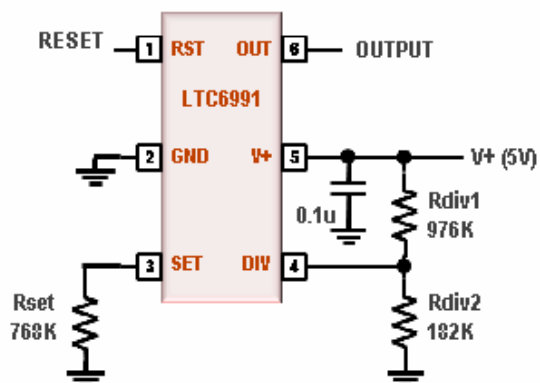


DEFAULT CIRCUIT CONFIGURATIONS FOR EACH VERSION

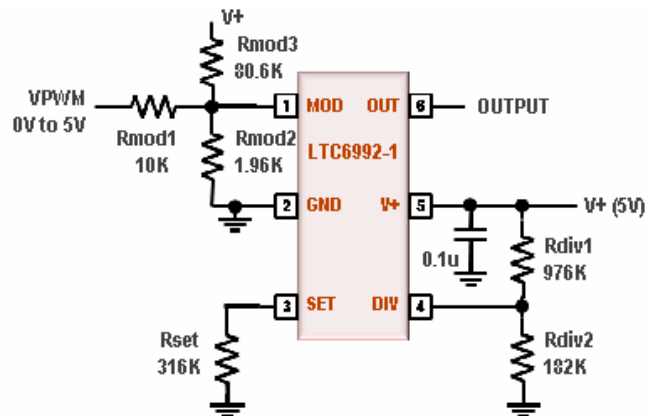
DC1652A-A, 1KHZ TO 10KHZ VCO



DC1652A-B, 1HZ (1SEC PERIOD) FIXED FREQUENCY OSCILLATOR



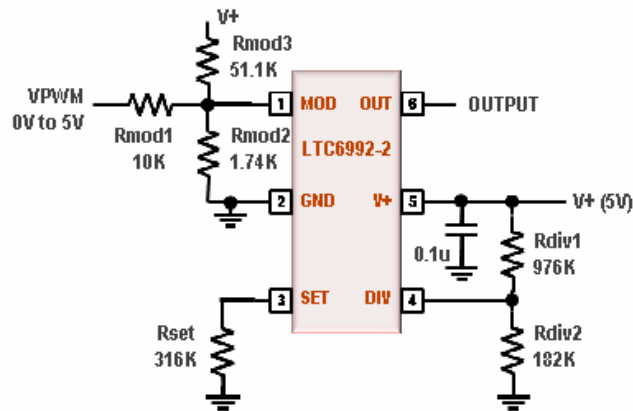
DC1652A-C, 10KHZ 0% TO 100% DUTY CYCLE PWM



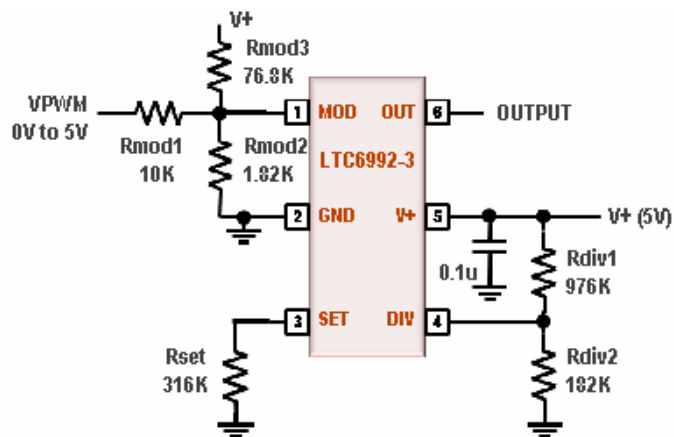
LTC699X

DEFAULT CIRCUIT CONFIGURATIONS FOR EACH VERSION

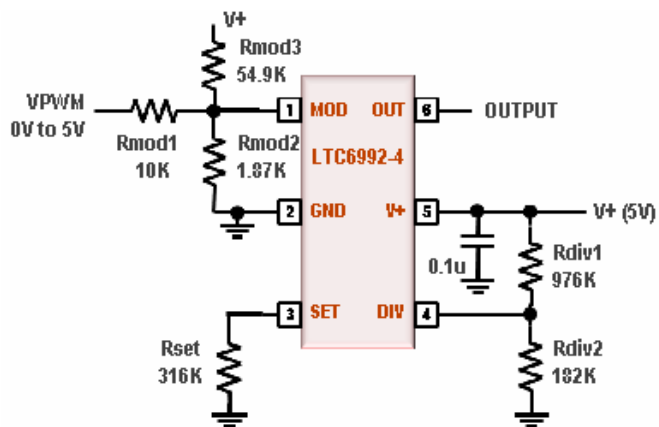
DC1652A-D, 10KHZ 5% TO 95% DUTY CYCLE PWM

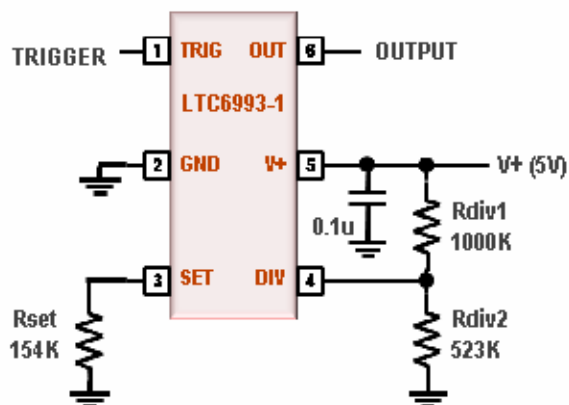
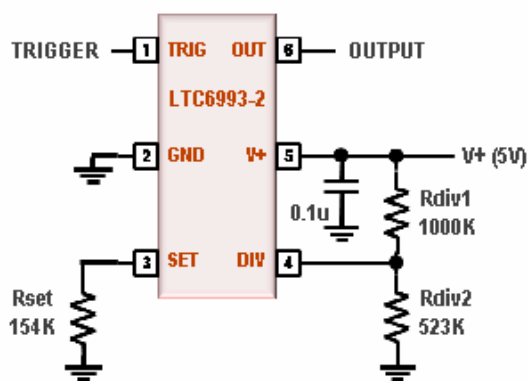
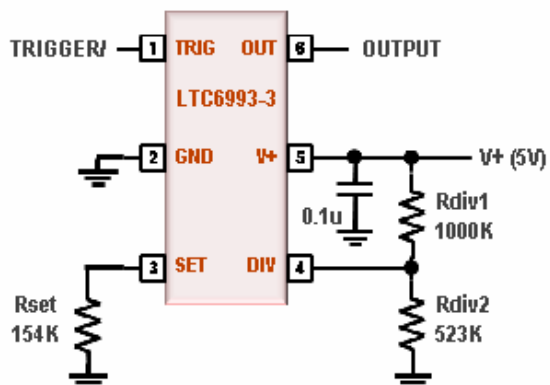


DC1652A-E, 10KHZ 0% TO 95% DUTY CYCLE PWM



DC1652A-F, 10KHZ 5% TO 100% DUTY CYCLE PWM

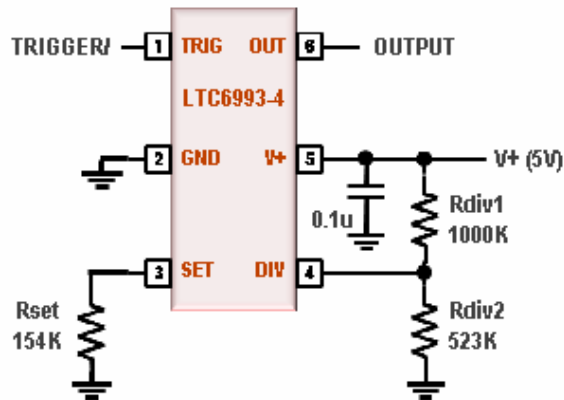


DEFAULT CIRCUIT CONFIGURATIONS FOR EACH VERSION
DC1652A-G, RISING EDGE TRIGGERED 100MS POSITIVE OUTPUT PULSE ONE SHOT**DC1562A-H, RISING EDGE RE-TRIGGERABLE 100MS POSITIVE OUTPUT PULSE ONE SHOT****DC1562A-I, FALLING EDGE TRIGGERED 100MS POSITIVE OUTPUT PULSE ONE SHOT**

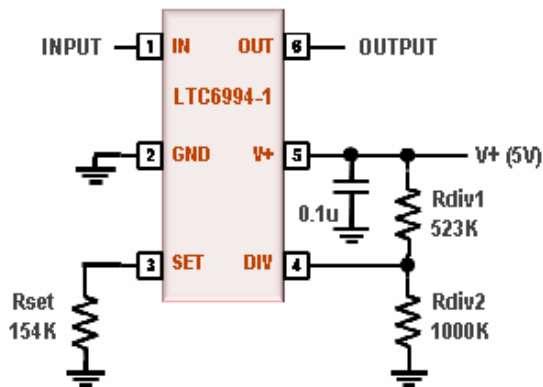
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DEFAULT CIRCUIT CONFIGURATIONS FOR EACH VERSION

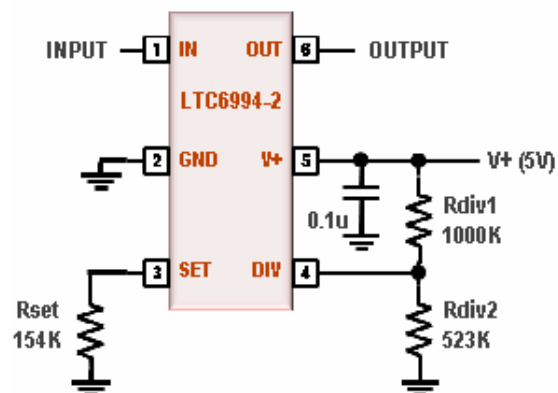
DC1562A-J, FALLING EDGE RE-TRIGGERABLE 100MS POSITIVE OUTPUT PULSE ONE SHOT



DC1562A-K, 100MS DELAYED OUTPUT FALLING EDGE FROM INPUT FALLING EDGE



DC1562A-L, 100MS DELAYED OUTPUT EDGE FROM INPUT EDGE, BOTH RISING AND FALLING EDGES



* VERSION TABLE

ASSY TYPE	U1	R1	R2	R3	R4	R5	R6	RSET	PSF
DC1562A-A	LTC699AES6	1M	801K	100K	0	OPEN	432K	95.3K	OE
DC1562A-B	LTC699IES6	978K	182K	OPEN	0	100K	OPEN	789K	RST
DC1562A-C	LTC699ES6-1	978K	182K	80.6K	10K	1.98K	OPEN	316K	MOD
DC1562A-D	LTC699ES6-2	978K	182K	51.1K	10K	1.74K	OPEN	316K	MOD
DC1562A-E	LTC699ES6-3	978K	182K	76.8K	10K	1.82K	OPEN	316K	MOD
DC1562A-F	LTC699ES6-4	978K	182K	54.9K	10K	1.87K	OPEN	316K	MOD
DC1562A-G	LTC699ES6-1	1M	520K	OPEN	0	100K	OPEN	154K	TRIG
DC1562A-H	LTC699ES6-2	1M	520K	OPEN	0	100K	OPEN	154K	TRIG
DC1562A-I	LTC699ES6-3	1M	520K	OPEN	0	100K	OPEN	154K	TRIG
DC1562A-J	LTC699ES6-4	1M	520K	OPEN	0	100K	OPEN	154K	TRIG
DC1562A-K	LTC699AES6-1	520K	1M	OPEN	0	100K	OPEN	154K	TRIG
DC1562A-L	LTC699AES6-2	1M	520K	OPEN	0	100K	OPEN	154K	TRIG

* STANDARD CONFIGURATIONS TABLE

ASSY TYPE	U1	CONFIGURED FUNCTION
DC1562A-A	LTC699AES6	1KHz to 10KHz VCO
DC1562A-B	LTC699IES6	1Hz (1 SEC) FIXED FREQUENCY
DC1562A-C	LTC699ES6-1	10KHz, 0 - 100% DUTY CYCLE
DC1562A-D	LTC699ES6-2	10KHz, 5 - 95% DUTY CYCLE
DC1562A-E	LTC699ES6-3	10KHz, 0 - 95% DUTY CYCLE
DC1562A-F	LTC699ES6-4	10KHz, 5 - 100% DUTY CYCLE
DC1562A-G	LTC699ES6-1	100ms ONE SHOT, RISING EDGE TRIGGERED
DC1562A-H	LTC699ES6-2	100ms RE-TRIGGERABLE (RISING EDGE) ONE SHOT
DC1562A-I	LTC699ES6-3	100ms ONE SHOT, FALLING EDGE TRIGGERED
DC1562A-J	LTC699ES6-4	100ms RE-TRIGGERABLE (FALLING EDGE) ONE SHOT
DC1562A-K	LTC699AES6-1	100ms OUTPUT FALLING EDGE DELAYED FROM TRIGGER FALLING EDGE
DC1562A-L	LTC699AES6-2	100ms OUTPUT RISING EDGE DELAYED FROM TRIGGER RISING EDGE

